IN THE CLAIMS

1. (Original) A MOSFET comprising:

a semiconductor substrate with a relatively thick first region and a relatively thin second region;

a gate insulating layer pattern formed on said first region of the semiconductor substrate;

a gate conductive layer pattern formed on the gate insulating layer pattern;

an epitaxial layer formed on said second region of the semiconductor substrate so as to have a predetermined thickness;

spacers formed on sidewalls of the gate conductive layer pattern and part of the surface of the epitaxial layer;

a lightly-doped first impurity region formed in the semiconductor substrate disposed below the spacers and in the epitaxial layer; and

a heavily-doped second impurity region formed in a portion of the semiconductor substrate, exposed by the spacers.

2. (Original) The MOSFET of claim 1, wherein the semiconductor substrate is a silicon substrate, and the epitaxial layer is a silicon epitaxial layer.

3. (Original) The MOSFET of claim 1, wherein the sum of the thickness of the epitaxial layer and the thickness of said second region is greater than the thickness of said first region.

4. (Original) The MOSFET of claim 1, wherein said first region has a first thickness, said second region has a second thickness, and the sum of the thickness of said epitaxial layer and said second thickness is greater than said first thickness.

5. (Original) The MOSFET of claim 4, wherein the thickness of the epitaxial layer ranges from approximately 20 to approximately 500 Å.

6. (Original) The MOSFET of claim 1, wherein the gate insulating layer pattern and the insulating layer are silicon oxide layers, and the gate conductive layer pattern is a polysilicon pattern.

7. (Original) The MOSFET of claim 1, wherein the spacers include double insulating layers.

8. (Original) The MOSFET of claim 1, wherein the thickness of the epitaxial layer ranges from approximately 20 to approximately 500 Å.

9. (Withdrawn) A method of fabricating a MOSFET, in which a gate insulating layer pattern, a gate conductive layer pattern, and a mask pattern are sequentially stacked on a first region of a semiconductor substrate, and a second region of the semiconductor substrate is recessed by a predetermined thickness during an etch process using the mask pattern for forming the gate insulating layer pattern and the gate conductive layer pattern, the method comprising:

forming a first insulating layer on the second region of the semiconductor substrate, the exposed sidewalls of the gate conductive layer pattern, and the exposed surface of the mask pattern;

forming a second insulating layer on the first insulating layer;

forming a first insulating pattern and a second insulating pattern by etching the first insulating layer and the second insulating layer so as to expose a top surface of the mask pattern and the remaining surface of the second region excluding part of the surface of the second region contacting the first region;

substantially completely exposing the second region by etching the first insulating layer so as to remove part of the surface of the first insulating pattern contacting the semiconductor substrate;

growing an epitaxial layer over the exposed second region;

removing the mask pattern, the second insulating pattern, and the first insulating pattern so as to expose a surface of the epitaxial layer and a top surface and sidewalls of the gate conductive layer pattern;

forming an ion implantation buffer layer on the exposed surface of the epitaxial layer and a surface of the gate conductive layer pattern;

forming a lightly-doped impurity region in the epitaxial layer and the semiconductor substrate by performing a first ion implantation process;

removing the ion implantation buffer layer so as to expose the lightly-doped impurity region and a top surface and sidewalls of the gate conductive layer pattern;

sequentially forming a third insulating layer and a fourth insulating layer on the exposed surfaces of the lightly-doped impurity region and the gate conductive layer pattern;

forming spacers by etching the third insulating layer and the fourth insulating layer so as to expose part of the surface of the epitaxial layer; and

forming a heavily-doped impurity region in the epitaxial layer and the semiconductor substrate by performing an ion implantation process using the spacers as an ion implantation mask.

10. (Withdrawn) The method of claim 9, wherein the second insulating layer is formed of a material having an etch selectivity with respect to the first insulating layer.

11. (Withdrawn) The method of claim 9, wherein the epitaxial layer is formed to a thickness of approximately 20 Å to approximately 200 Å.

12. (Withdrawn) A method of fabricating a MOSFET on a semiconductor substrate with a relatively thick first region and a relatively thin second region;

forming a gate insulating layer pattern on said first region of said semiconductor substrate;

forming a gate conductive layer pattern on the gate insulating layer pattern;

forming an epitaxial layer on said second region having a predetermined thickness;

forming a lightly-doped first impurity region in the semiconductor substrate disposed below the spacers and in the epitaxial layer;

forming spacers on sidewalls of the gate conductive layer pattern and part of the surface of the epitaxial layer; and

forming a heavily-doped second impurity region in a portion of the semiconductor substrate, exposed by the spacers.

13. (Withdrawn) The method of claim 12, wherein the semiconductor substrate is a silicon substrate, and the epitaxial layer is a silicon epitaxial layer.

14. (Withdrawn) The method of claim 12, wherein said first region has a first thickness, said second region has a second thickness, and the sum of the thickness of said epitaxial layer and said second thickness is greater than said first thickness.

15. (Withdrawn) The method of claim 14, wherein the thickness of the epitaxial layer ranges from approximately 20 to approximately 500 Å.

16. (Withdrawn) The method of claim 12, wherein the gate insulating layer pattern and the insulating layer are silicon oxide layers, and the gate conductive layer pattern is a polysilicon pattern.

17. (Original) A MOSFET comprising:

a semiconductor substrate with a relatively thick first region and a relatively thin second region;

a gate insulating layer pattern formed on said first region of the semiconductor substrate;

a gate conductive layer pattern formed on the gate insulating layer pattern;

an epitaxial layer formed on said second region of the semiconductor substrate so as to have a predetermined thickness, the sum of the thickness of said epitaxial layer and the thickness of said second region being greater than the thickness of said first region;

spacers formed on sidewalls of the gate conductive layer pattern and part of the surface of the epitaxial layer;

a lightly-doped first impurity region formed in the semiconductor substrate disposed below the spacers and in the epitaxial layer; and

a heavily-doped second impurity region formed in a portion of the semiconductor substrate, exposed by the spacers.

18. (Original) The MOSFET of claim 17, wherein the thickness of the epitaxial layer ranges from approximately 20 to approximately 500 Å.

19. (Original) The MOSFET method of claim 17, wherein the gate insulating layer pattern and the insulating layer are silicon oxide layers, and the gate conductive layer pattern is polysilicon.

20. (Withdrawn) The method of fabricating a MOSFET as recited in claim 12 wherein a gate insulating layer pattern, a gate conductive layer pattern, and a mask pattern are sequentially stacked on said first region of said semiconductor substrate, and said second region of said semiconductor substrate is recessed by a predetermined thickness during an etch process using said mask pattern for forming said gate insulating layer pattern and the gate conductive layer pattern.

21. (Withdrawn) The method of fabricating a MOSFET as recited in claim 20 wherein said method includes forming a first insulating layer on the second region of the semiconductor substrate, the exposed sidewalls of the gate conductive layer pattern, and the exposed surface of the mask pattern.

22. (Withdrawn) The method of fabricating a MOSFET as recited in claim 21 wherein said method includes forming a second insulating layer on the first insulating layer;

forming a first insulating pattern and a second insulating pattern by etching the first insulating layer and the second insulating layer so as to expose a top surface of the mask pattern and the remaining surface of the second region excluding part of the surface of the second region contacting the first region;

substantially completely exposing the second region by etching the first insulating layer so as to remove part of the surface of the first insulating pattern contacting the semiconductor substrate;

growing said epitaxial layer over the exposed second region; and

removing said mask pattern, the second insulating pattern, and the first insulating pattern so as to expose a surface of the epitaxial layer and a top surface and sidewalls of the gate conductive layer pattern.

23. (Withdrawn) The method of fabricating a MOSFET as recited in claim 22 wherein said method includes forming said lightly-doped impurity region in the epitaxial layer and the semiconductor substrate by performing a first ion implantation process;

removing the ion implantation buffer layer so as to expose the lightly-doped impurity region and a top surface and sidewalls of the gate conductive layer pattern;

sequentially forming a third insulating layer and a fourth insulating layer on the exposed surfaces of the lightly-doped impurity region and the gate conductive layer pattern;

forming said spacers by etching the third insulating layer and the fourth insulating layer so as to expose part of the surface of the epitaxial layer; and

forming said heavily-doped impurity region in the epitaxial layer and the semiconductor substrate by performing an ion implantation process using said spacers as an ion implantation mask.